IN THE SPECIFICATION:

Please amend paragraph [0033] as is set forth below.

[0033] The structure of the demodulator is shown in Fig. 3. The down-converter output is sampled by the module 62 at ~~$f_s \geq 4R_s$~~ $f_s \geq 4R_s$ samples per second, where R_s is the symbol rate. The signal in the in-phase channel is filtered by the filter 64, which is matched to the pulse shaping filter if the impulse response of the power amplifier is unknown, or matched to the convolution of the pulse shaping function and the impulse response of the power amplifier. The signal in the quadrature channel is filtered by the filter 66, which is also matched to the pulse shaping filter if the impulse response of the power amplifier is unknown, or matched to the convolution of the pulse shaping function and the impulse response of the power amplifier. The correlator 68 and the correlator 70 correlate the received signal with the preamble in each packet for packet detection and parameter estimation. The packet detector 72 detects each packet. The parameter estimator 74 estimates the symbol time, the carrier phase and the frequency offset. The tracking loop 76 is initialized using the symbol time estimate, the carrier phase estimate and the frequency offset estimate. At the tracking loop output, the errors are minimized for symbol time, carrier phase and frequency offset.